CLAIMS

1. A method of π/4-shift QPSK modulation comprising:

addressing symbols from a Precursor section of a register to a first memory portion and from a Postcursor section of said register to a second memory portion at odd times, and

addressing symbols from said Precursor section to said second memory portion and from said Postcursor section to said first memory portion at even times by using reversed addressing for Postcursor symbols in accessing the said first and second memory portions.

2. The method of claim 1, further comprising:

successively incrementing the address indicated by the Precursor section of the register by a number of storing locations equal to said predetermined number of samples, and successively decrementing the address indicated by the Postcursor section of the register by a number of storing locations equal to said predetermined number of samples.

3. The method of claim 2, wherein the first memory portion and the second memory portion are adapted to Look Up Tables format.

4. The method of claim 3, wherein the shift register is adapted to comprise *n* symbols, the Precursor comprises n/2 of said symbols and the Postcursor comprises the remaining n/2 symbols.

5. The method of claim 4, wherein *n* being an even number.

6. The method of claim 4, further comprises

defining a transfer function of the modulator by an array of characteristic coefficients;

computing for each possible inputted symbol sequence, a predetermined number of sample values, said sample values being the sum of the products of said symbol sequence multiplied by said coefficients; and

providing an output of said modulator by an addition of the Precursor sum-of-products and Postcursor sum-of-products.

7. The method of claim 6, comprises:

storing said sums-of-products said first memory portion and said second memory portion.

8. The method of claim 7, comprises

defining an amplitude value of symbols inputted at odd times by combinations of an at least two bits and an amplitude value of symbols inputted at even times by an at least one bit, and feeding the resulting symbols to said shift register.

9. The method of claim 8, wherein a symbol comprising a number of predetermined samples.

10. The method of claim 1, further comprising:

assigning one symbol in the Precursor section and one symbol in the Postcursor section as sign symbols to said sections correspondingly; and

forming the address to the corresponding memory portion from the symbols coming from the corresponding register in accordance with the sign of said sign symbols.

11. The method of claim 10, wherein each of said sign symbols is selected from the symbols represented by one bit.

12. The method of claim 11, further comprising:

when a sign bit is negative, forming the address to the corresponding memory portion from all symbols coming from the corresponding register section except the sign symbol, reversing the sign of each symbol in the corresponding register section, and further reversing the sign of the outputs from the corresponding memory portion;

otherwise forming the address to the corresponding memory portion from all symbols coming from the corresponding register section except the sign symbol.

13. The method of claim 12, wherein the first and second memory portions are integrated in a single memory unit.

14. An $\pi/4$-shift QPSK modulator comprsing:

at least one shift register comprises at least one Precursor section and at least one Postcursor section;

at least one address convertor which is adapted to convert the symbols from the Precursor section of said register alternately to a first

and a second memory portions and from the Postcursor section of said register alternately to said second and first memory portions.

15. The modulator of claim 14, further comprises:

at least one counter adapted to increment and decrement the least significant bits of the address;

a plurality of multiplexers adapted to select the Precursor section of the register to form an address to the first memory portion, and the Postcursor section of the register to form an address to the second memory portion, while reversing the order of the Postcursor symbols, said selection is alternated at even and odd times.

16. The modulator of claim 15, further comprises:

at least one adder adapted to add a data outputted from said first memory portion to a data outputted from said second memory portion; and

at least one digital to analog convertor adapted to convert the combined output to an analog output.

17. The modulator of claim 15, wherein said second memory portion is adapted to integrate with unused memory locations of said first memory portion.

18. The modulator of claim 18, wherein the addresses in the memory are defined by a high address factor - Most Significant Bits, being formed by symbols in the register, and by a low address factor-Least Significant Bits, which generates in accordance with the order of sampling within the symbol.

19. The modulator of claim 18 wherein, said low address are provided by said counter.

20. The modulator of claim 14, wherein the at least one address converter comprises a plurality of multiplexers and gates for providing Most Significant Bits from the Precursor section into the first or second memory portion, and from the Postcursor section to the second or first memory portion accordingly.

21. The modulator of claim 16 wherein, the at least one counter is adapted to provide the Least Significant Bits of the address comprises an oversampling counter.

22. The modulator of claim 15, further comprising:

a bits to symbols conversion unit for converting a sequence of bits into a sequence of symbols represented alternately by one and two bits.

23. The modulator of claim 22, wherein said shift register is adapted to receive said sequence of symbols.